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EXAMINER	
ELMORE, REBA I	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/644,695	SOROUSHI, ATOUSA	
	Examiner	Art Unit	
	Reba I. Elmore	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,10-18,21-29,32,33,37-41 and 43-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,10-18,21-29,32,33,37-41 and 43-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 10-18, 21-29, 32-33, 37-41 and 43-50 are presented for examination.

SPECIFICATION

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

35 USC § 102

3. The rejection of claims 1-7, 10-18, 21-29, 32-33 and 37-41 as being anticipated by Wollan et al. is ***maintained*** and repeated below with changes to include the amendments to the claims and the newly added claims.

4. The following is a quotation of the appropriate paragraphs of 35 USC 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-7, 10-18, 21-29, 32-33, 37-41 and 43-50 are rejected under 35 USC 102(b) as being anticipated by Wollan et al. (P/N 5,809,327).

6. Claims 1-7, 10-18, 21-29, 32-33 and 37-41 are rejected under 35 USC 103(a) as being unpatentable over Wollan et al. (P/N 5,809,327).

7. Wollan teaches the invention (claim 1) as claimed including a method for high speed addressing of a memory space having 2^M addresses using an N-Bit bus, where M is greater than N, the method comprising:

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(a) providing at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus as the 16 bit logical registers (e.g., see Figure 1, element 20);

(b) receiving a first address-byte on the bus as receiving the first half of an address directed to one of the double address registers (e.g., see col. 4, line 62 to col. 5, line 20);

(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte as the system keeping track of the first half of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct address register (e.g., see col. 4, line 62 to col. 5, line 20);

(d) selecting a first one of the at least two registers, the first register corresponding with the first count as selecting the 16 bit double registers rather than the 8 bit registers (e.g., see col. 4, line 47 to col. 5, line 20);

(e) storing the first address-byte in the selected first register as receiving the first half of an address directed to one of the double address registers (e.g., see col. 4, line 62 to col. 5, line 20).

As to claim 2, Wollan teaches receiving a second address-byte; producing a second count of address bytes received on the bus as a result of receiving the second address-byte; selecting a second one of the two registers, the second register corresponding with the second count and storing the second address-byte in the selected second register (e.g., see col. 4, line 47 to col. 5, line 20).

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As to claim 3, Wollan teaches receiving a memory access command and accessing the memory space at an address defined by the first and second address-bytes as a result as the 16 bit logical registers (e.g., see Figure 1, element 20).

As to claim 43, Wollan teaches the write command transfers data on the N-bit bus

As to claims 4-5, Wollan teaches the memory access command as read or write commands (e.g., see col. 7, lines 49-60).

As to claim 44, Wollan teaches the read command transfers data on the N-bit bus

As to claims 6-7, Wollan teaches the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte and the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte (e.g., see col. 5, line 6-47).

As to claims 10-11, Wollan teaches providing at least two memories, wherein the 2^M address memory space comprises the address space of the memory (e.g., see col. 1, lines 38-57).

8. Wollan teaches the invention (claims 12-13) as claimed including an apparatus for high speed addressing of a memory space having 2^M addresses comprising:

(a) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus as the 16 bit logical registers (e.g., see Figure 1, element 20);

(b) an N-bit bus, where M is greater than N (e.g., see col. 1, lines 38-57);

(c) first and second control signal lines as having a plurality of control signal lines (e.g., see Figure 1);

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(d) a logic circuit coupled with the bus, the first and second control signal lines and the two registers, the logic circuit to select one of the two registers as the logic circuitry (a program counter, program flash, instruction register and instruction decoder shown in Figure 1) for using either an 8 bit address register or the 16 bit logical registers of the register file (e.g., see Figure 1, element 20), the logic circuit including:

(i) a K-bit address–byte-received counter to count address bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal line, wherein the number of at least two registers is less than or equal to 2^K and receiving one byte of the plurality of N-bit bytes that together define an address in the memory space as the system keeping track of the first half of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct address register (e.g., see col. 4, line 62 to col. 5, line 20);

(ii) a selecting unit to select one of the two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the two registers for a particular count value of the address-byte-received counter as the system keeping track of the second half of the logical address (e.g., see col. 4, line 62 to col. 5, line 20).

As to claim 14, Wollan teaches the apparatus further comprises a unit to receive a memory access command and a access the memory space at an address defined by the first and second address-bytes as a result of the memory access command (e.g., see Figure 1).

As to claims 15-16, Wollan teaches the memory access command as read or write commands (e.g., see col. 7, lines 49-60).

As to claims 17-18, Wollan teaches the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte and the unit receives the

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memory access command in a next subsequent bus transaction following receipt of the second address-byte (e.g., see col. 5, line 6-47).

As to claims 21-22, Wollan teaches providing at least two memories, wherein the 2^M address memory space comprises the address space of the memory (e.g., see col. 1, lines 38-57).

As to claims 45-46, Wollan teaches K can equal one or two

9. Wollan teaches the invention (claim 23) as claimed including a machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus, where M is greater than N, the program method comprising:

(a) receiving a first address-byte on the bus as receiving the first half of a logical address (e.g., see col. 4, line 62 to col. 5, line 5);

(b) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte as a result of tracking the use of logical addressing as receiving the first half of a logical address (e.g., see col. 4, line 62 to col. 5, line 5);

(c) selecting a first of the two registers, the first register corresponding to the first count as the first or upper register of the 16 bit logical address register (e.g., see col. 4, line 62 to col. 5, line 5); and,

(d) storing the first address-byte in the selected first register (e.g., see col. 4, line 62 to col. 5, line 5).

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As to claim 24, Wollan teaches the method further comprising receiving a second address-byte; producing a second count of address-bytes received on the bus as a result of receiving the second address-byte; selecting a second one of the two registers with the second register corresponding with the second count and storing the second address-byte in the selected second register as using indirect addressing for the logical addressing (e.g., see Table III and col. 13, lines 1-40).

As to claim 25, Wollan teaches receiving a memory access command and accessing a memory at an address defined by the first and second address-bytes as a result of the memory access command (e.g., see col. 14, lines 46-65).

As to claims 26-27, Wollan teaches the memory access command as read or write commands (e.g., see col. 14, lines 39-65).

As to claims 28-29, Wollan teaches the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte (e.g., see col. 5, line 6-47 and col. 14, lines 46-65).

As to claim 32, Wollan teaches providing at least two memories, wherein the 2^M address memory space comprises the address space of the memory (e.g., see col. 1, lines 38-57).

As to claims 47-48, Wollan teaches the write access and read access transfers data on the N-bit bus

10. Wollan teaches the invention (claim 37) as claimed including a system comprising:

(a) an N-bit bus, where M is greater than N (e.g., see col. 1, lines 38-57);

(b) a memory having 2^M addresses (e.g., see col. 1, lines 38-57);

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(c) a central processing unit, coupled to the bus, to transmit at least two address-bytes that together define an address in the memory space and to transmit a memory access command (e.g., see Figure 1);

(d) at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory, each register associated with a particular count of address-bytes received on the bus as the 16 bit logical registers (e.g., see Figure 1, element 20);

(e) first and second control signal lines as a plurality of control signal lines (e.g., see Figure 1);

(f) a logic circuit coupled with the bus, the first and second control signal lines and the two registers as the logic circuitry (a program counter, program flash, instruction register and instruction decoder shown in Figure 1) for using either an 8 bit address register or the 16 bit logical registers of the register file (e.g., see Figure 1, element 20), the logic circuit including:

(i) a K-bit address-bye-receiver counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal ling, wherein the number of at least two registers is less than or equal to 2^K as the system keeping track of the first half of the 16 bit logical address otherwise the system would not place the second half of the 16 bit logical address in the correct address register (e.g., see col. 4, line 62 to col. 5, line 20);

(ii) a selecting unit to select one of the two registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct one of the two registers for a particular count value of the address-byte-received counter as the system keeping track of the second half of the logical address (e.g., see col. 4, line 62 to col. 5, line 20).

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(g) a unit to:

(i) receive the memory access command (e.g., see Figure 1); and,

(ii) access the memory at an address defined by the first and second address-bytes as a result of the memory access command (e.g., see Figure 1).

As to claims 38-39, Wollan teaches the memory access command as read or write commands (e.g., see col. 14, lines 39-65).

As to claims 40-41, Wollan teaches the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte wherein the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte (e.g., see col. 5, line 6-47 and col. 14, lines 46-65).

As to claims 43-50, Wollan teaches K can equal one or two as the system being capable of utilizing different numbers of address bytes dependent upon whether direct address or indirect addressing is used for either read commands or write commands (e.g., see Figure 1 and col. 4, line 47 to col. 5, line 53).

11. The rejection of claims 1-7, 10-18, 21-29, 32-33 and 37-41 as being anticipated by Potter et al. is ***maintained*** and repeated below with changes to include the amendments to the claims and the newly added claims.

12. Claims 1-7, 10-18, 21-29, 32-33 and 37-42 are rejected under 35 USC 102(b) as being anticipated by Potter et al. (P/N 5,170,477).

13. Potter teaches the invention (claim 1) as claimed including a method for high speed addressing of a memory space having 2^M addresses using an N-Bit bus, where M is greater than N, the method comprising:

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(a) at least two registers as a buffer of temporary registers (e.g., see Figure 1, element 20), each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus (e.g., see col. 3, line 53 to col. 4, line 30);

(b) receiving a first address-byte on the N-bit bus as the DMA controller having input and output buses (e.g., see Figure 1);

(c) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte as the DMA controller (e.g., see Figure 1, element 10) which determines the first address of the amount of data being requested (e.g., see col. 3, line 53 to col. 4, line 30);

(d) selecting a first register which corresponds to the first count as the selecting the registers within the buffer for a selected memory operation (e.g., see col. 3, line 53 to col. 4, line 30); and,

(e) storing the first address-byte in the selected first register (e.g., see col. 4, lines 37-59).

As to claim 2, Potter teaches receiving a second address-byte as a second data item for temporary storage in the buffer; producing a second count of address bytes received on the bus as a result of receiving the second address-byte; selecting a second register corresponding to the second count and storing the second address-byte i the selected second register as receiving and storing data items in the second register of the buffer with the counter keeping count of the data items (e.g., see col. 3, line 53 to col. 4, line 30).

As to claim 3, Potter teaches receiving a memory access command and accessing the memory space at an address defined by the first and second address-bytes as a result of the memory access command as programming functions including data transfers directed to the DMA controller for accessing memory devices (e.g., see col. 2, line 51 to col. 3, line 24).

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As to claims 4-5, Potter teaches the memory access command can be read commands or write commands as memory device accesses including data transfers (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 6-7, Potter teaches the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte and the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte as a first address-byte for the memory command being followed by the second address-byte dependent upon the address size of the memory device (e.g., see Figure 1 and col. 3, line 53 co col. 4, line 30).

As to claims 10-11, Potter teaches at least two memory devices are used for the 2^M address memory space (e.g., see Figure 5).

14. Potter teaches the invention (claim 12-13) as claimed including an apparatus for high speed addressing of a memory space having 2^M addresses comprising:

(a) at least two registers as a buffer of temporary registers (e.g., see Figure 1, element 20), each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus (e.g., see col. 3, line 53 to col. 4, line 30);

(b) an N-bit bus, where M is greater than N (e.g., see Figure 5);

(c) first and second control signal lines (e.g., see Figure 1);

(d) a logic circuit coupled with the bus, the first and second control signal lines and the registers, the logic circuit to select one of the two registers as the DMA controller being programmable (e.g., see Figure 1 and col. 3, lines 53-63);

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(i) a K-bit address–byte-received counter to count address bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal line, wherein the number of the two registers is less than or equal to 2^K as the reference teaching using different size buses for data transfers (e.g., see Figure 1, element 40); and,

(ii) a selecting unit to select one of the registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct registers for a particular count value of the address-byte-received counter as gating circuitry (e.g., see Figure 1, element 30).

As to claim 14, Potter teaches receiving a memory access command and accessing the memory space at an address defined by the first and second address-bytes as a result of the memory access command as programming functions including data transfers directed to the DMA controller for accessing memory devices (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 15-16, Potter teaches the memory access command can be read commands or write commands as memory device accesses including data transfers (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 17-18, Potter teaches the second address-byte is received in a next subsequent bus transactions following receipt of the first address-byte and the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte as a first address-byte for the memory command being followed by the second address-byte dependent upon the address size of the memory device (e.g., see Figure 1 and col. 3, line 53 to col. 4, line 30).

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As to claims 21-22, Potter teaches at least two memory devices are used for the 2^M address memory space (e.g., see Figure 5).

15. Potter teaches the invention (claim 23) as claimed including a machine readable medium embodying a program of instructions for execution by a machine to perform a method for high speed addressing of a memory space having 2^M addresses using an N-bit bus, the machine having at least two registers, each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus, where M is greater than N (e.g., see Figure 1), the steps comprising:

(a) receiving a first address-byte on the N-bit bus of the DMA controller having input and output buses (e.g., see Figure 1);

(b) producing a first count of address-bytes received on the bus as a result of receiving the first address-byte as the DMA controller (e.g., see Figure 1, element 10);

(c) selecting a first register which corresponds to the first count as the selecting the registers within the buffer of a selected memory operation (e.g., see col. 3, line 53 to col. 4, line 30); and,

(d) storing the first address-byte in the selected first register (e.g., see col. 4, lines 37-59).

As to claim 24, Potter teaches receiving a second address-byte as a second data item for temporary storage in the buffer; producing a second count of address-bytes received on the bus as a result of receiving the second address-byte; selecting a second register corresponding to the second count and storing the second address-byte in the selected second register as receiving and storing data items in the second register of the buffer with the counter keeping count of the data items (e.g., see col. 3, line 53 to col. 4, line 30).

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As to claim 25, Potter teaches receiving a memory access command and accessing a memory space at an address defined by the first and second address-bytes as a result of the memory access command as programming functions including data transfers directed to the DMA controller for accessing memory devices (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 26-27, Potter teaches the memory access command can be read commands or write commands as memory device accesses including data transfers (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 28-29, Potter teaches the second address-byte is received in a next subsequent bus transaction following receipt of the first address-byte and the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte as a first address-byte for the memory command being followed by the second address-byte dependent upon the address size of the memory device (e.g., see Figure 1 and col. 3, line 53 to col. 4, line 30).

As to claims 32-33, Potter teaches the 2^M address memory space comprises the address space of a memory

As to claim 33, Potter teaches at least two memory devices are used for the 2^M addressable memory space (e.g., see Figure 5).

16. Potter teaches the invention (claim 37) as claimed including a system comprising:

(a) an N-bit bus, where M is greater than N (e.g., see Figure 5);

(b) a memory having 2^M addresses (e.g., see col. 2, lines 39-48);

(c) a central processing unit (e.g., see col. 1, lines 14-20), coupled to the bus, to transmit at least two address-bytes that together define an address in the memory space and to transmit a

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memory access command as programming functions including data transfers directed to the DMA controller for accessing memory devices (e.g., see col. 2, line 51 to col. 3, line 24);

(d) at least two registers as a buffer of temporary registers (e.g., see Figure 1, element 20), each register to store a distinct N-bit address-byte of a plurality of address-bytes that together define an address in the memory space, each register associated with a particular count of address-bytes received on the bus (e.g., see col. 3, line 53 to col. 4, line 30);

(e) first and second control signal lines (e.g., see Figure 1);

(f) a logic circuit coupled with the bus, the first and second control signal lines, and the registers, the logic circuit to select one of the registers as the DMA controller being programmable (e.g., see col. 3, lines 53-63);

(i) a K-bit address-bye-receiver counter to count address-bytes received on the bus by counting each assertion of an address transfer signal on the first control signal line when a write signal is asserted on the second control signal line, wherein the number of the two registers is less than or equal to 2^K as the reference teaching using different size buses for data transfers (e.g., see Figure 1, element 40);

(ii) a selecting unit to select one of the registers according to the count of the address-byte-received counter, wherein the selecting unit selects a distinct register for a particular count value of the address-byte-received counter (e.g., see Figure 1, element 30); and,

(g) a unit to:

(i) receive the memory access command (e.g., see col. 2, lines 51-62); and,

(ii) access the memory at an address defined by the first and second address-bytes as a result of the memory access command (e.g., see col. 2, line 51 to col. 3, line 24).

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As to claims 38-39, Potter teaches the memory access command can be read commands or write commands as memory device accesses including data transfers (e.g., see col. 2, line 51 to col. 3, line 24).

As to claims 40-41, Potter teaches the logic circuit receives a second address-byte in a next subsequent bus transaction following receipt of a first address-byte and the memory access command is received in a next subsequent bus transaction following receipt of the second address-byte as a first address-byte for the memory command being followed by the second address-byte dependent upon the address size of the memory device (e.g., see Figure 1 and col. 3, line 53 to col. 4, line 30).

As to claim 42, Potter teaches the system is capable of being used in a wide variety of devices including a cellular telephone or any device or method using a CPU (e.g., see col. 12, line 66 to col. 13, line 2), particularly as usage of an invention cannot predicate patentability. Neither the claims, drawings now specification provide any details which support a particular usage of the present invention to the degree necessary to allow patentability to be tied to the use itself.

As to claims 43-50, Potter teaches K can equal one or two as the system being capable of utilizing different numbers of address bytes dependent upon whether direct address or indirect addressing is used for either read commands or write commands (e.g., see Figures 1-10).

RESPONSE TO APPLICANY'S REMARKS

17. Applicant's arguments filed September 20, 2007 have been fully considered but they are not persuasive.

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18. As to Wollan not teaching a counter for counting address bytes received, the Wollan system uses registers as either 8 bit registers or 16 bit registers. In order for the system to utilize the pairs of 16 bit registers, the first byte is counted as the first half of the total 16 bit address.

19. As to the references not teaching the claims to the extent required for applying the references as anticipating the claimed elements, the claimed limitations are taught to the extent required by the actual claim language. In fact, the background of the present invention describes indirect addressing such as that taught in both references as being a two part activity. The references not mentioning a counter specifically does not mean this is not the more common method of performing such a two part step such as indirect addressing. The specific mention of a counter in the claims does not make the claims patentable as this is a common, necessary piece of hardware found in all addressing structures. This argument is similar to demanding the reference state the memory elements comprise silicon material or buses or transistors.

20. As to the reference incrementing the content of a logical register not being equivalent to incrementing a count whenever a byte is received, the claim language does not state that every byte is counted or give any additional details of which bytes are counted. The reference teaching any counting of address bytes meets the broad recitation of the actual claim language.

21. As to claim 37 requiring both registers and a memory, the figures of the reference clearly show both a wide variety of registers being used as well as different types of memory devices being part of the invention as taught by Wollan.

22. As to the Potter reference not teaching an N-bit bus, Potter teaches buses of different sizes in the background of the invention. The Potter reference also keeps track of the amount of data to be transferred just as is common in all such systems. The data transfer would not be

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performed if the hardware was not in place for the amount of the data transfer to be tracked. This is fundamental in memory systems.

OFFICE ACTION FINALITY

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

CONCLUSION

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reba I. Elmore, whose telephone number is (571) 272-4192. The examiner can normally be reached on Monday and Thursday from 7:30am to 6:00pm, EST. If attempts to reach the examiner by telephone are unsuccessful, the art unit supervisor for AU 2189, Reginald G. Bragdon, can be reached for general questions concerning this application at (571) 272-4204. Additionally, the official fax phone number for the art unit is (571) 273-8300.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center central telephone number is (571) 272-2100.

Reba I. Elmore
Primary Patent Examiner
Art Unit 2189

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